Measurement - Based Extrinsic Modeling of RF Components

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Abstract: **An understanding of the high-frequency parasitic and packaging effects of passive surface-mounted devices (SMDs) is required for robust equivalent circuit modeling of the device. In this paper, we develop a CAD model for SMD inductors on a CPW layout, which incorporates the non-ideal behavior associated with frequency dispersion, board layout, component parasitics, and the device packaging. The equivalent circuit parameters are extracted in closed-form from an accurate measurement of the S-parameters of the board-mounted SMD inductor, without the necessity for cumbersome optimization procedures normally followed in RF circuit synthesis.**

I. INTRODUCTION

Passive surface-mounted devices, such as thin-film inductors, capacitors and resistors, are extensively employed in the RF industry. These components are wave-soldered or wire-bond onto associated pads on a printed circuit board. At radio frequencies, the combination of component packaging, pad footprint, PCB layout and the substrate interaction causes detrimental local parasitic effects, such as resonant coupling, signal loss, signal distortion, etc. Circuit modeling of these devices should therefore consider the environment in which the devices will be operated, a process henceforth termed as *extrinsic modeling*.

Synthesis of equivalent circuit models for discrete components usually involves either electromagnetic simulations or measurements, followed by curve-fitting the resulting data to the response of a desired model, chosen on the basis of designer's *a priori* knowledge of the component [1] – [3]. Automation of the curve-fitting process entails complex optimization routines, and thus becomes unmanageable except for simple circuit configurations. There are two main disadvantages in using global optimization to develop equivalent circuit models. First, it is impractical in such an optimizer to accurately evaluate the frequency dependence (dispersion, loss, etc.) of the model, since the process yields frequency-independent, ideal elements. Second, the complex geometrical attributes such as packaging and novel materials demand co-simulation between 3D simulators and optimizers. This requires considerable computer resources, and even then, it becomes difficult to ensure that the optimization indeed converged to the correct solution. To circumvent this optimization process, some authors have attempted to synthesize equivalent circuits in closed-form, valid at either low frequencies or over a narrow frequency range, where dispersion and loss mechanisms are not predominant (e.g. [4]). These closed-form expressions also yield constant element values, albeit valid over a narrow frequency-band. In summary, the usually wide-band layout- and package-specific parasitic effects are not considered in these CAD models.

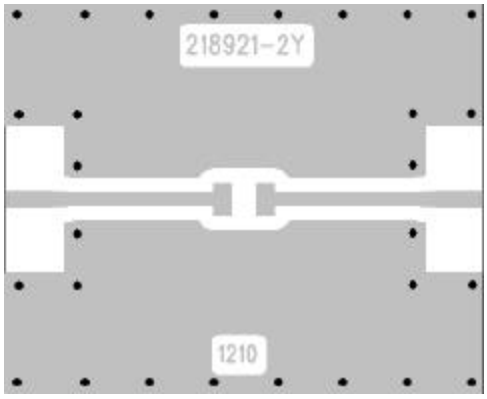

Fig. 1. CPW pad and trace configuration for an SMD component. The pad edges on the feed lines define reference planes.

This paper seeks to develop a comprehensive, frequency-dependent equivalent circuit model of SMD inductors, starting from broadband S-parameter measurements of the inductor on a Network Analyzer (NA). The inductor is mounted in a grounded CPW fixture representing the circuit environment of the application. The impedance mismatch between the fixture and the NA is error-corrected by direct calibration at a reference plane located at the edge of the component footprint (see Fig. 1), using Short, Open, Load and Thru (SOLT) calibration standards developed specifically for the CPW environment. Thus, the resulting circuit model exclusively captures the sought-after interaction (parasitics) between the PCB environment and the component. Such models can potentially reduce the number of design iterations in a practical situation, since the model is based on accurate *in-situ* measurements tied to the application environment. Besides, as we discuss in the next section, these extrinsic models also improve the accuracy of circuit simulations.

0-7803-6540-2/01/$10.00 (C) 2001 IEEE

II. Equivalent Circuit Synthesis

A. *Extrinsic vs Intrinsic Modeling*

Component models supplied by the manufacturer, or those derived from measurements on LCR meters, bridges and impedance analyzers, describe the intrinsic characteristics of the component, and therefore, preclude package and layout parasitics associated with the motherboard and the circuit housing. By definition, an *intrinsic* circuit model does not include these parasitic effects, whereas an *extrinsic* model does. Intrinsic specifications are of limited value in design. Besides being inaccurate, designing a circuit based on the nominal value provided by the intrinsic model inevitably leads to considerable tuning and testing after board fabrication. With reference to Fig. 1, if an SMD inductor is mounted between the pads, the board parasitics significantly change the inductor circuit model derived from intrinsic measurements. Thus the parasitic effects of different layouts may result in different resonant frequencies and Q-factors for the same inductor.

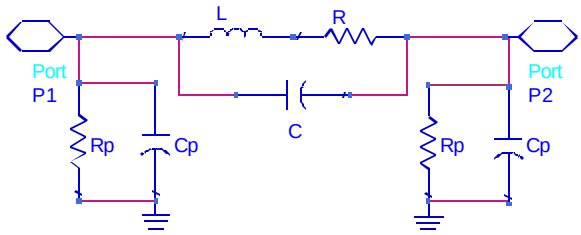

Fig. 2. Two-port extrinsic equivalent circuit model for inductor.

The augmented extrinsic circuit model of the SMD inductor is shown in Fig. 2. The series resistance R includes the SMD package losses, skin and proximity effects, as well as the pad or trace losses. Likewise, the series capacitance C represents the self-capacitance of the inductor package and the capacitance between the pads. The pad is simply a step-in-width, inductive transition, and augments the series inductance of the intrinsic model. The total inductance is denoted as L. The dielectric losses in the substrate introduce a shunt conductance $G_p = 1/R_p$, and the capacitance to ground of each pad introduces a shunt C_p, which is also influenced by the substrate. It is evident that the resonant frequency and Q of the intrinsic RLC model are altered by parasitic loading. We assume that the operating wavelength is large enough for the parasitics to be considered local to the SMD component.

If we base the design on the extrinsic circuit model, the increased accuracy attained by incorporating board parasitics can potentially reduce the number of design cycles. Furthermore, using an accurate library base of extrinsic equivalent circuit models, it is feasible to accomplish most of the design-centering on a circuit simulator instead of the bench.

B. *Closed-Form Inductor Model*

The direct measurement of the model parameters, L, R and C, of a surface mounted inductor is difficult because of their strong interaction with the board parasitics. Typically, any of these parameters can be obtained indirectly from measurable parameters such as impedance, quality factor and resonant frequency. In this research, we measure the S-parameters of an SMD inductor in a CPW environment using a Vector Network Analyzer, with on-board calibration done at the reference planes shown in Fig. 1. We now describe how one can synthesize the equivalent circuit, shown in Fig. 2, from these measurements. The synthesis is accomplished in closed-form without the cumbersome numerical procedures (e.g., optimization) usually involved in obtaining physical device parameters from RF measurements.

Denoting the series impedance in Fig. 2 as Z and the shunt admittance as Y_p, we have

$$Z = \frac{R + j\omega L}{1 - \omega^2 LC + j\omega RC} \tag{1}$$

$$Y_p = G_p + j\omega C_p \tag{2}$$

The ABCD matrix of the circuit in Fig. 2 is given by

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} ZY_p + 1 & Z \\ Y_p(ZY_p + 2) & ZY_p + 1 \end{bmatrix} \tag{3}$$

We note that this matrix represents the measured S-parameters through the appropriate transformations. Thus, the left-hand-side of (3) is known at each measured frequency, and the objective is to compute the equivalent circuit elements in Fig. 2 *as functions of frequency*. First, we note that

$$Z(\omega) = B(\omega) \tag{4}$$

$$Y_p(\omega) = \frac{A(\omega) - 1}{B(\omega)} \tag{5}$$

Since $A = D$ and $AD - BC = 1$ (reciprocal network), there are only two independent parameters in the chain matrix. Thus, there are two equations available in (3) to synthesize the circuit model in Fig. 2. From (5), we calculate the shunt conductance and capacitance as

$$G_p = \mathrm{Re}(Y_p) \tag{6}$$

$$C_p = \frac{\mathrm{Im}(Y_p)}{2\pi f} \tag{7}$$

The series impedance $Z(\omega)$ in (4) presents two (real) equations to determine the three variables, L, R and C. $Z(\omega)$ resonates at the frequency ω_0 with a quality factor Q, both of which can be obtained explicitly from the measured parameter, $B(\omega)$. The resonant frequency is determined as the frequency at which $\mathrm{Im}(B) = 0$, and Q is computed from the observed 3-dB bandwidth. The impedance $Z(\omega) = Z_r(\omega) + jZ_i(\omega)$ in (1) may then be written as

$$Z(\omega) = \frac{R + j\omega L^2 C(\omega_0^2 - \omega^2)}{(1-\omega^2 LC)^2 + (\omega RC)^2} \tag{8}$$

At the resonant frequency, let Z_0 (real) be the impedance, and $Q = \omega_0 L_0 / R_0$ be the quality factor. L_0 and R_0 are the inductance and the resistance at resonance, and may be calculated as:

$$R_0 = \frac{Z_0}{1+Q^2} \tag{9}$$

$$L_0 = \frac{QR_0}{\omega_0} \tag{10}$$

The capacitance of SMD inductors is practically independent of frequency, and follows from:

$$C = \frac{1}{\omega_0^2 L_0} \frac{Q^2}{1+Q^2} \tag{11}$$

After some algebra, the frequency-dependent inductance and resistance can be obtained in closed-form as:

$$L(\omega) = \frac{Z_1 Z_2}{\omega(Z_1 + Z_2)} \tag{12}$$

$$R(\omega) = \frac{Z_r(\omega)\left[1 - A\dfrac{\omega L(\omega)}{R_0}\right]}{1 + A\dfrac{Z_i(\omega)}{R_0}} \tag{13}$$

$$Z_1 = \frac{R_0}{A}, \quad Z_2 = \frac{A\,|Z(\omega)|^2 + R_0 Z_i(\omega)}{R_0 + AZ_i(\omega)}, \tag{14}$$

$$A = \frac{\omega}{\omega_0}\frac{Q}{1+Q^2}. \tag{15}$$

These expressions are adequate for modeling SMD inductors at frequencies below the second resonance. At these frequencies, the distributed effects of the equivalent circuit model can be neglected. Besides modeling SMD inductors, we have used (12) to compute the effective permeability of wide-band ferrite chokes utilized in EMI suppression.

III. Sample Results

The example pertains to the measured data for a Coilcraft 68 nH ceramic inductor, mounted on IEC 1210 SMD pad footprint. Fig. 3 displays the magnitude of S21. The dip in transmission corresponds to parallel resonance between the inductor packaging and the pad layout.

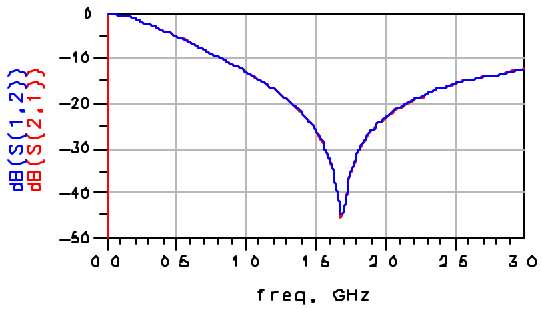

Fig. 3. Magnitude (dB) of S21 for a 68 nH SMD inductor.

In order to determine the resonant frequency and Q more accurately, we convert the S-parameters to the *ABCD* parameters. The magnitude and phase of B are shown in Fig. 4. The resonant frequency and Q at resonance are calculated from the magnitude curve. The peak resistance is about 25 kΩ. It is clear that the reactance is predominantly inductive below the resonant frequency and capacitive above that frequency.

For comparison, we have also measured the same component using HP 4291 Impedance Analyzer with HP 16191 SMD Test Fixture, and plotted the result in Fig. 4. This instrument measures only the intrinsic characteristics of the component; hence, it does not capture the interaction between board layout and component. The NA measurement does include layout effects. Comparing the two measurements for the resonant frequency and Q summarized in Table I (first number in each cell), we observe that the discrepancy is about 13% in resonant frequency and 48% in Q. Incidentally, because of parasitic loading, both Q's are lower than the value (55 at 300 MHz) reported in *Coilcraft's March 1998 Catalog*.

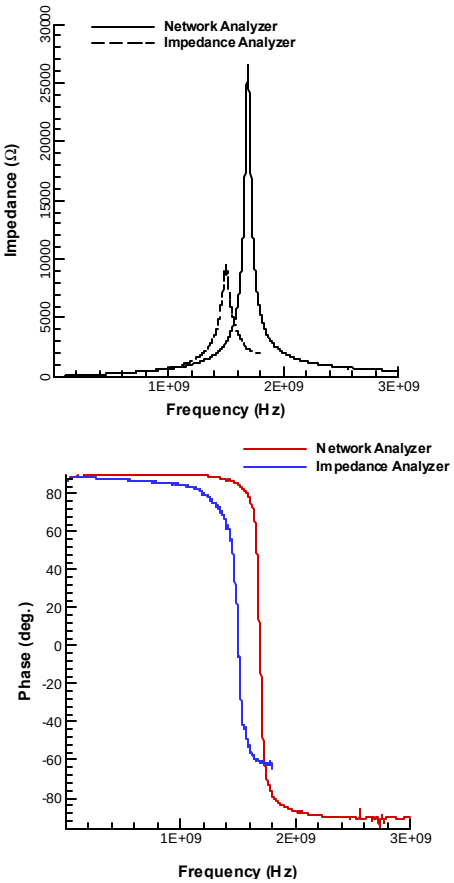

Fig. 4. Comparison of (a) magnitude and (b) phase of the impedance measured using the NA and the HP 4291 Impedance Analyzer. The maximum frequency of HP 4291 is 1.8 GHz.

We repeated the two measurements with another sample of the same nominal value (68 nH). Table I also depicts the resonant frequency and Q for this replicate (the second number in each cell). The discrepancy between the two samples (batch variation, tolerance, etc.) is evident.

TABLE I: CHARACTERISTICS OF TWO REPLICATES MEASURED ON TWO INSTRUMENTS.

Instrument	f_0 (GHz)	Q
HP 8753	1.689, 1.632	39.10, 35.49
HP 4291	1.497, 1.520	20.45, 17.44

The inductance and resistance of the SMD package are shown in Fig. 5. The inductance lies between 71 nH and 67 nH up to the resonant frequency, where it dips abruptly and changes to a capacitance of 0.14 pF (calculated using eq. (11)). The resistance varies from $0.25\,\Omega$ at 1 MHz to 1 $k\Omega$ at resonance. The shunt conductance and capacitance are not plotted for brevity. The conductance G_p is negligible ($<1\,m\Omega$), while the capacitance C_p remains between 0.25 pF and 0.4 pF.

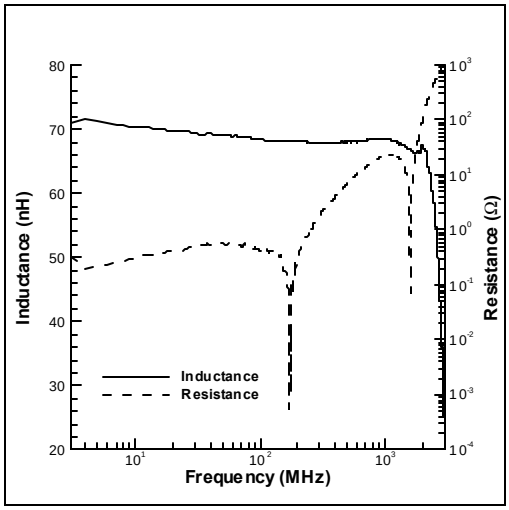

Fig. 5. Inductance and resistance of the 68 nH SMD package.

IV. CONCLUSION

We have presented a method to derive extrinsic equivalent circuit models, which consider the parasitics of the design environment, such as layout and package effects, material loss, etc. The model is derived in closed-form from S-parameters measured on a Network Analyzer, without using any numerical optimization, normally followed in RF circuit synthesis. We have demonstrated the procedure for SMD inductors, focusing on the advantages of extrinsic over intrinsic modeling. It is anticipated that the increased accuracy attained by incorporating layout/package parasitic effects will allow for easier design-centering and reduce the design cycles.

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